I. IN THE CLAIMS:

Claims 1, 4, 11, 16, 19 and 24 are amended, and claims 9-10, 14, and 22 are cancelled, as follows:

Listing of Claims

1. (Currently Amended) A method, comprising:

[[~~generating a checkpoint at one of a plurality of branches in a checkpoint buffer having at least one checkpoint buffer entry~~]]

identifying from a plurality of branches a low confidence branch;

assigning to the low confidence branch a checkpoint and counter information about the checkpoint in a checkpoint buffer, wherein said plurality of branches include one or more instructions;

[[~~generating a counter for said at least one checkpoint buffer entry;~~]] associating said one or more instructions with said checkpoint; and

tracking with said counter said one or more instructions associated with said checkpoint.

2. (Originally Filed) The method of claim 1, further comprising: accessing said checkpoint at the occurrence of a recovery event; restoring an architectural state associated with said checkpoint; and processing at least one instruction from said one or more instructions associated with said checkpoint.

3. (Originally Filed) The method of claim 1, further comprising: reclaiming said checkpoint when said counter indicates that said one or more instructions associated with said checkpoint have been completed.

4. (Currently Amended) The method of claim 1, said [[generating a checkpoint]] identifying a low confidence branch further comprising: estimating a misprediction probability for one or more of said plurality of branches.

5. (Originally Filed) The method of claim 1, wherein generating said checkpoint occurs when a checkpoint buffer entry is available.

6. (Originally Filed) The method of claim 1, further comprising processing beyond said plurality of branches without generating said checkpoint when said checkpoint buffer entry is not available.

7. (Originally Filed) The method of claim 1, wherein said tracking step further comprises: incrementing said counter when said one or more instructions is allocated; and decrementing said counter when said one or more instructions completes execution.

8. (Originally Filed) The method of claim 1, wherein checkpoints are reclaimed in a first-in-first-out order.

Claims 9-10. (Cancelled).

11. (Currently Amended) An apparatus, comprising:

a branch confidence estimator to identify a low confidence branch from a plurality of branches;

a branch predictor to [~~generate~~] assign a checkpoint [[~~at one of a plurality of branches~~]] to the identified low confidence branch;

and a checkpoint buffer to store one or more counters, wherein said checkpoint buffer has at least one checkpoint buffer entry; wherein said branch predictor generates a counter for said at least one checkpoint buffer entry to associate one or more instructions with said checkpoint, and wherein said branch predictor tracks said one or more instructions using said counter.

12. (Originally Filed) The apparatus of claim 11, wherein said branch predictor accesses said checkpoint at the occurrence of a recovery event, restores an architectural state associated with said checkpoint, and processes at least one instruction from said one or more instructions associated with said checkpoint.

13. (Originally Filed) The apparatus of claim 11, wherein said branch predictor reclaims said checkpoint when said counter indicates that said one or more instructions associated with said checkpoint have been completed.

Claim 14 (Cancelled).

15. (Originally Filed) The apparatus of claim 14, wherein said branch confidence estimator accesses misprediction history information.

16. (Currently Amended) The apparatus of claim 15, wherein said branch confidence estimator further comprises a counter associated with said low confidence branch [[~~having a high misprediction probability~~]] and adapted to track when said branch is mispredicted.

17. (Originally Filed) The apparatus of claim 11, further comprising: a recovery buffer to store previously executed instructions for use in misprediction recovery.

18. (Originally Filed) The apparatus of claim 11, wherein said branch predictor further comprises a branch target buffer to store said one or more instructions.

19. (Currently Amended) A system, comprising:

a processor including a branch confidence estimator to identify a low confidence branch from a plurality of branches and a branch predictor to [[~~generate~~]] assign a checkpoint at [[~~one of a plurality of branches~~]] the identified low confidence branch, and a checkpoint buffer to store one or more counters, wherein said checkpoint buffer has at least one checkpoint buffer entry, wherein said branch predictor generates a counter for said at least one checkpoint buffer entry to associate one or more instructions with said assigned checkpoint, and wherein said branch predictor tracks said one or more instructions using said counter;

an interface to couple said processor to input-output devices; and

a data storage coupled to said interface to receive code from said processor.

20. (Originally Filed) The system of claim 19, wherein said branch predictor accesses said checkpoint at the occurrence of a recovery event, restores an architectural state associated with said checkpoint, and processes at least one instruction from said one or more instructions associated with said checkpoint.

21. (Originally Filed) The system of claim 19, wherein said branch predictor reclaims said checkpoint when said counter indicates that said one or more instructions associated with said checkpoint have been completed.

Claim 22 (Cancelled).

23. (Originally Filed) The system of claim 22, wherein said branch confidence estimator accesses misprediction history information.

24. (Currently Amended) The system of claim 23, wherein said branch confidence estimator further comprises a counter associated with the assigned low confidence branch [[~~said branch having a high misprediction probability~~]] and adapted to track when said branch is mispredicted.

25. (Originally Filed) The system of claim 19, further comprising: a recovery buffer to store previously executed instructions for use in misprediction recovery.

26. (Originally Filed) The system of claim 19, wherein said branch predictor further comprises a branch target buffer to store said one or more instructions.